ABSTRACT

A system is provided for independently testing a circuit module embedded in a larger integrated circuit, such as a system of a chip. The system uses essentially the circuit board level JTAG standard originally created to test chips mounted on a circuit board. The system provides a scan ring for serially scanning data to the inputs of the circuit module and for serially scanning out output from the circuit module. A test access port provides communications and control from an off-chip test interface to the scan rings.